Notice of References Cited	Application/Control No. 09/966,412	Applicant(s)/Patent Under Reexamination FORD, RICHARD L.	
	Examiner Tuan A Vu	Art Unit 2124	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,598,221	07-2003	Pegatoquet et al.	717/152
	B	US-6,467,082	10-2002	D'Arcy et al.	717/127
	C	US-5,574,927	11-1996	Scantlin, Henry L.	712/41
	D	US-5,815,720	09-1998	Buzbee, William B.	717/158
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Meerwein et al., "Embedded Systems Verification with FPGA-Enhanced In-Circuit Emulator", Sept. 2000, Proceedings of the 13th International Symposium on System Synthesis, ISSS 00, pp. 143-148
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.